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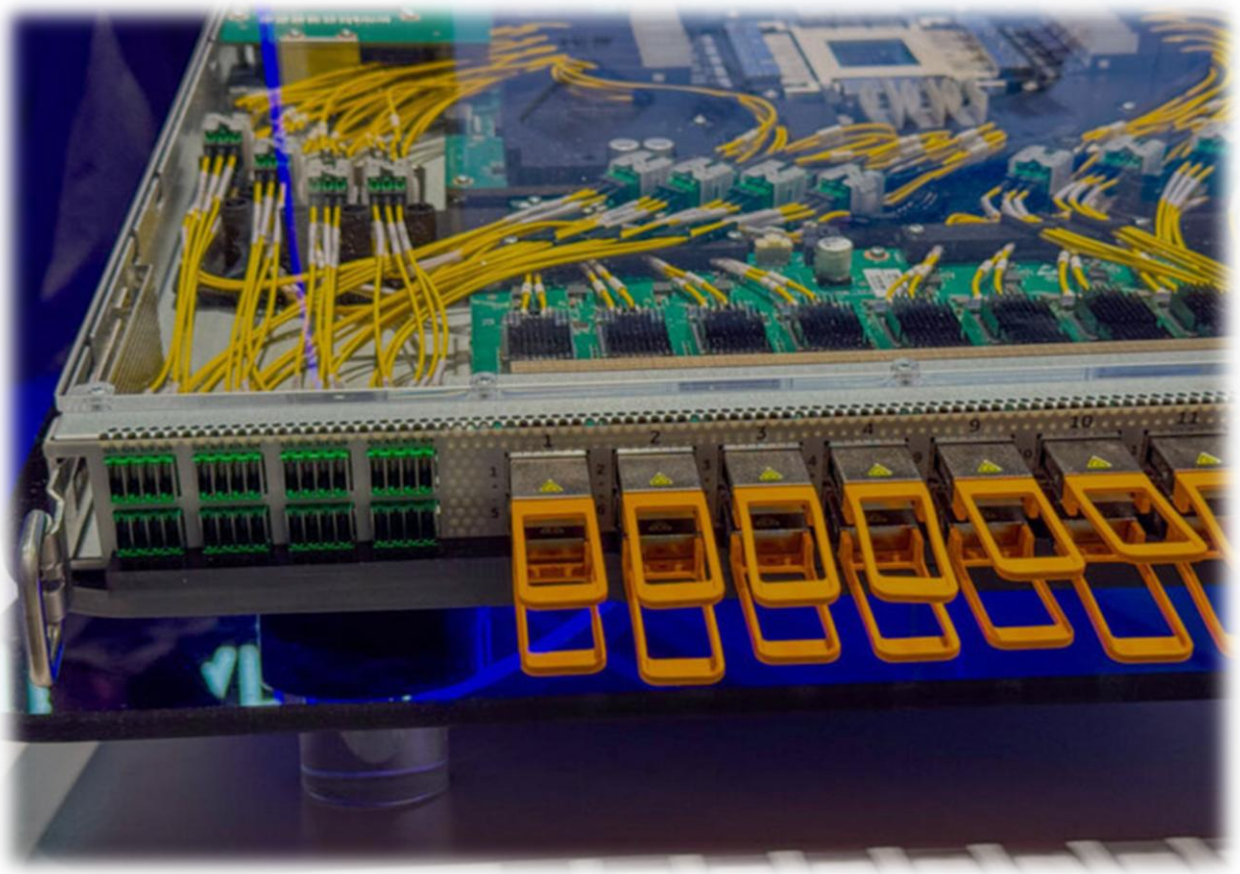

— THEMATIC RESEARCH · AI INFRASTRUCTURE

Co-Packaged Optics 101

The future of high-density AI interconnects

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— EXECUTIVE SUMMARY

The largest architectural change in data-centre networking in a decade

KEY TAKEAWAYS

- **The copper wall is here.** Above ~200Gbps per lane, copper can no longer carry signals more than a few metres without prohibitive power and signal-integrity penalties. The industry's answer is to move the optics off the faceplate and onto the chip package itself — **Co-Packaged Optics (CPO)**.
- **Adoption is switch-first.** NVIDIA and Broadcom are shipping CPO switches in 2026 on external-laser designs; the XPU side and an in-package laser are deferred by packaging and reliability limits, not yet solved.
- **Money moves with the architecture.** As the optical engine moves into the package, value migrates away from module assemblers toward the layers that fabricate the optical engine itself.

AI compute is colliding with a physical limit: above 200Gbps per lane, copper can no longer carry signals more than a few metres without prohibitive power and signal-integrity penalties. The industry's answer is to move the optics from a pluggable module at the faceplate onto the chip package itself — Co-Packaged Optics (CPO). At GTC 2026 and subsequentially COMPUTEX 2026, CPO crossed from show-floor demonstrations to a headline architecture for the next generation of AI infrastructure. This report explains why that transition is now structural rather than speculative (Sections 1–3), how the technology generations will roll out and in what order the market will adopt them (Section 4), who actually builds the supply chain and where the investable value concentrates (Section 5), how Singapore is involved (Section 6) and what could derail the adoption (Section 7).

WHY THIS MATTERS FOR INVESTORS

CPO is the largest architectural change in data-centre networking in over a decade, and architectural changes redistribute value. As the optical engine moves into the package, value migrates away from module assemblers toward wafer-level photonics, advanced packaging, and a small number of sole-source component choke points. Public forecasts for the CPO market range from **~$100m in 2025 to between $10bn and nearly $40bn in 2030**, depending on how far CPO is implemented into future builds.

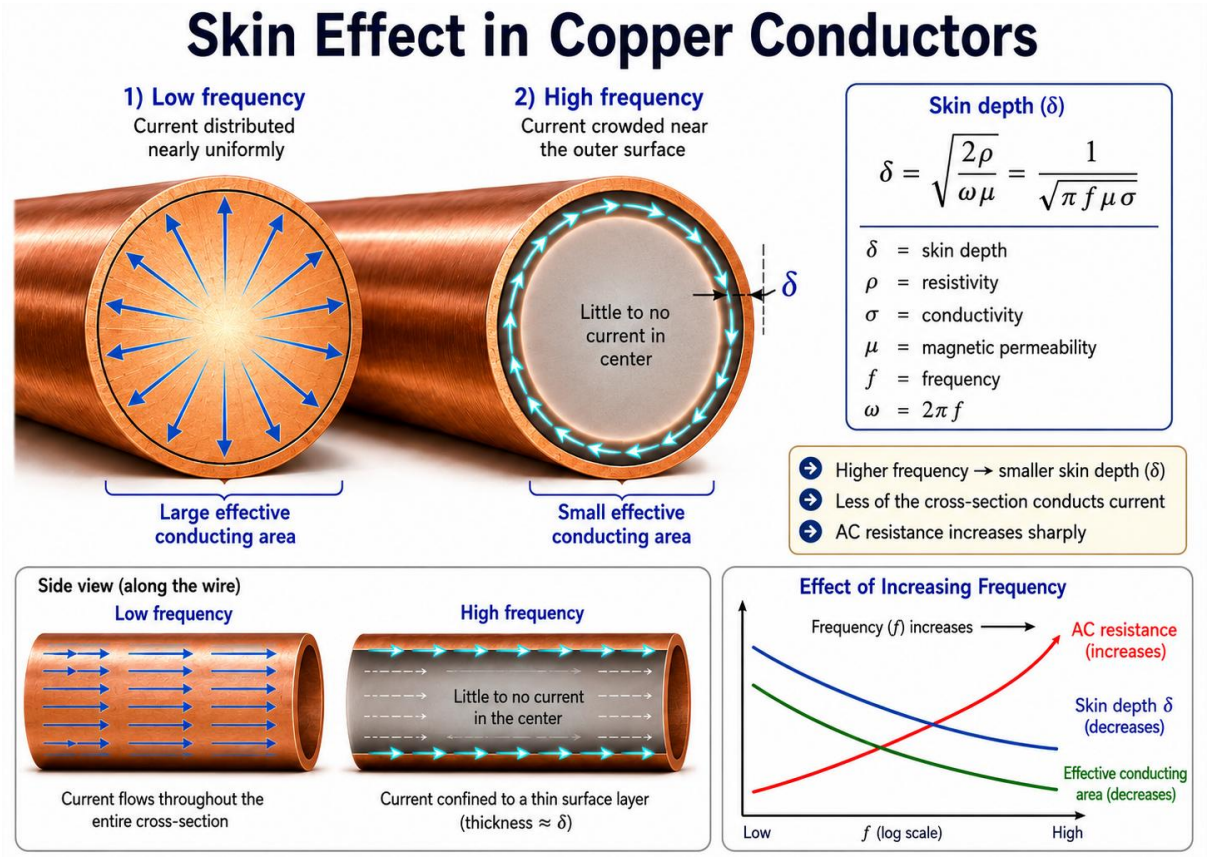
WHAT THIS REPORT COVERS

01 THE IMPENDING COPPER WALL

Why Optics is inevitable

The semiconductor industry has entered a "physics-limited" era where the scaling of AI compute - exemplified by Nvidia's Blackwell and Rubin architectures - is colliding with the material constraints of traditional electrical interconnects. For decades, copper-based Direct Attach Copper (DAC) cables were the gold standard, leading to Jensen Huang's mantra: "use copper wherever you can, and use optics only where you must." But as per-lane data rates migrate toward 200Gbps and 400Gbps, the industry is hitting the copper wall.

AI-ready data centres with such high transmission speeds physically require ultra-high analog frequencies exceeding 50 GHz. At these frequencies, copper's insertion loss and signal degradation become prohibitive beyond a few metres - a strategic bottleneck for the scale-out and scale-up requirements of 100k+ GPU clusters. Traditional copper links suffer two physical failure modes that make error-free recovery nearly impossible without extreme power overhead:



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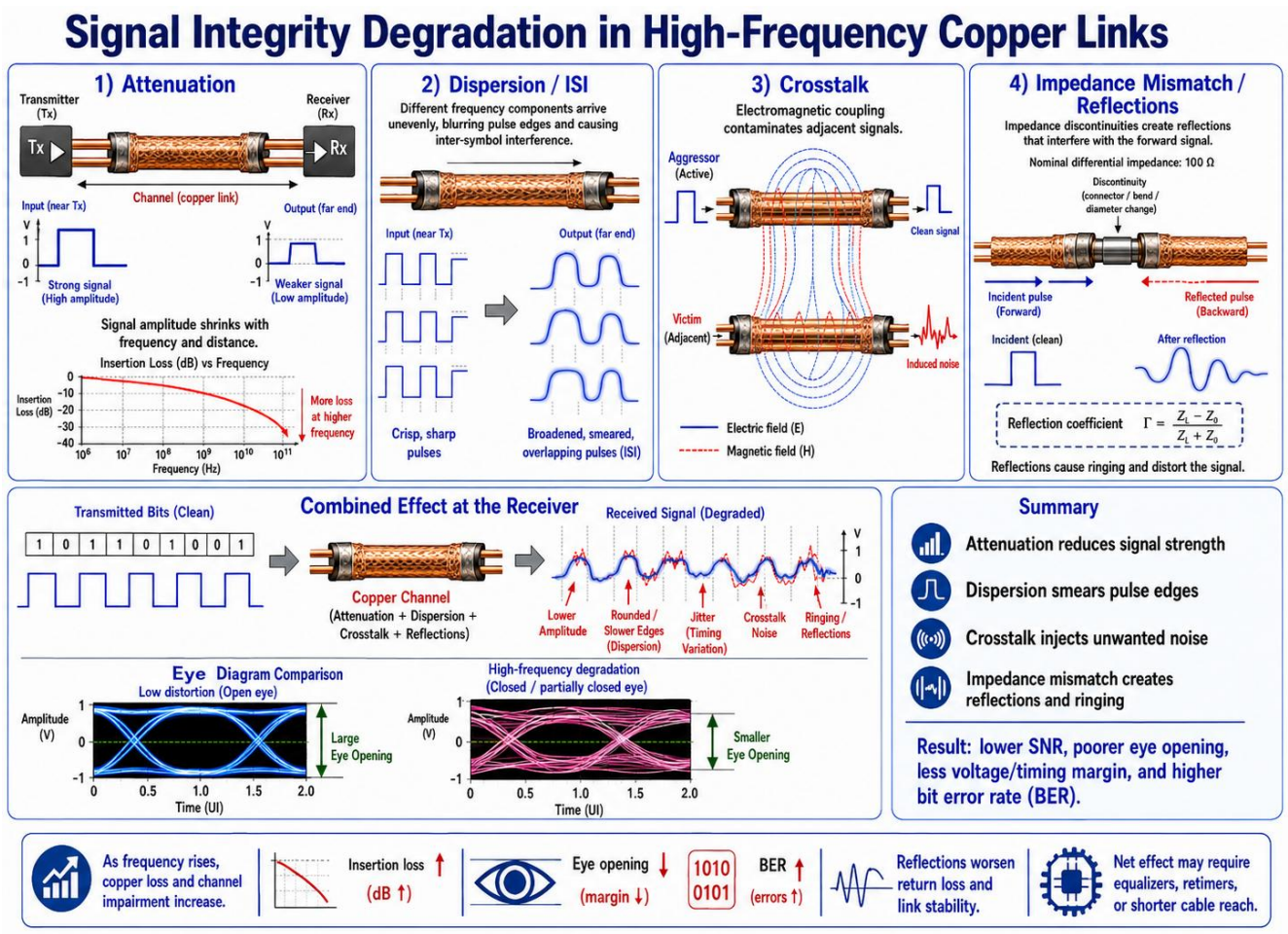
The Skin Effect: As signal frequencies increase, current is forced toward the conductor's surface, effectively reducing the cross-sectional area available for electron flow. This reduction in effective cross-section raises the cable's AC resistance, resulting in higher insertion loss where more signal power converts to heat. One industry solution has been to make thicker copper cables to increase the net effective conducting area, but there are physical constraints. Thicker copper cables become heavier, stiffer, harder to route, worse for airflow, and impractical in high-density data-centre environments.



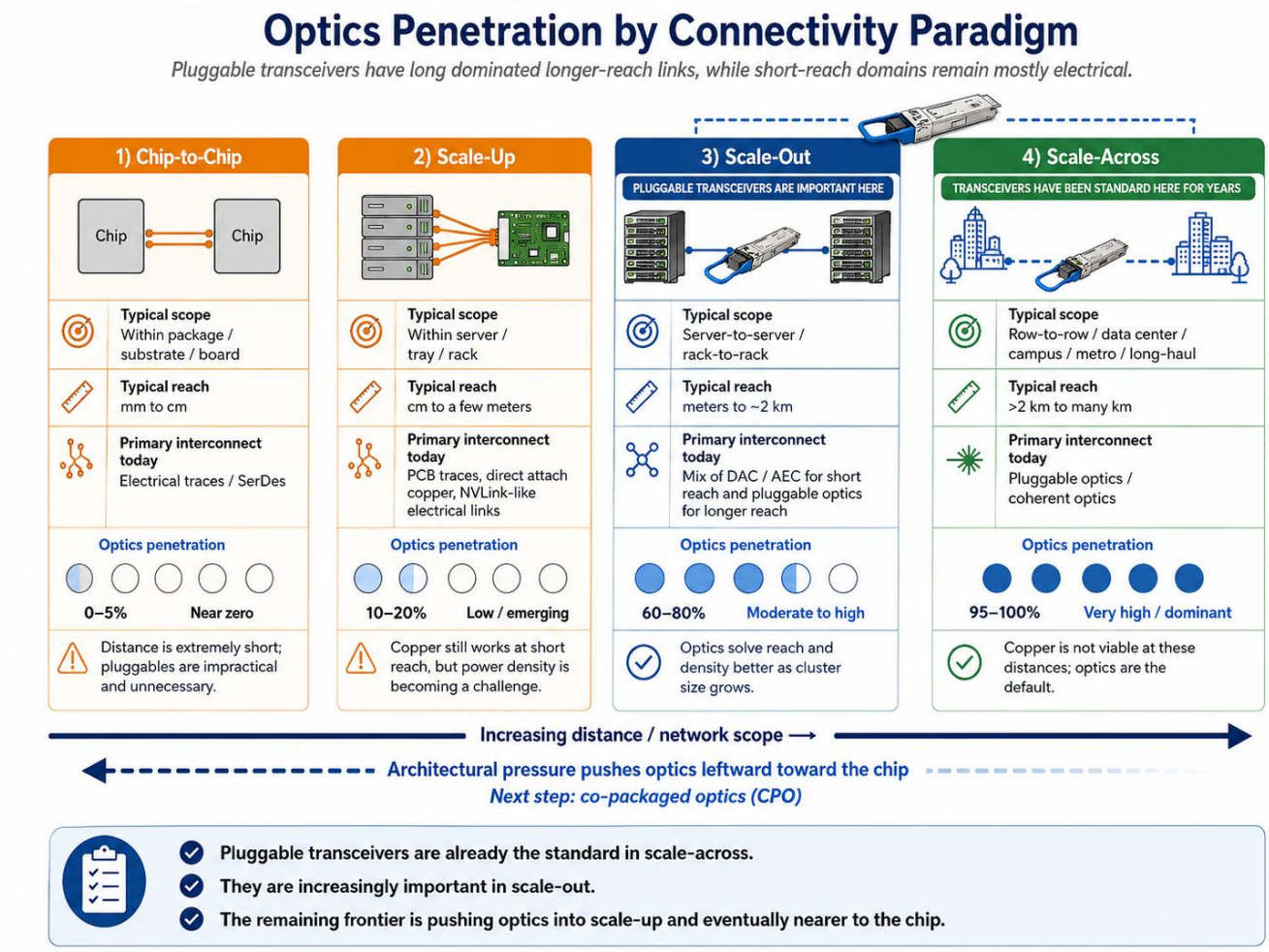
Source: AI-generated (ChatGPT, OpenAI, May 2026). For illustrative purposes only.

Signal Integrity Degradation: High-frequency copper links are plagued by attenuation, dispersion, crosstalk and impedance mismatch. Attenuation weakens the signal as frequency and distance increase, while dispersion causes different frequency components to arrive at slightly different times, smearing pulse edges and creating inter-symbol interference. Crosstalk occurs when electromagnetic fields leak between adjacent twinax pairs, contaminating the victim signal with unwanted noise. Impedance mismatch adds another source of distortion: any connector transition, bend, diameter change, or other geometric discontinuity can disrupt the cable's controlled differential impedance, causing part of the signal to reflect backward and interfere with the forward-traveling waveform.

Together, the received signal becomes weaker, noisier, and/or less sharply timed. The receiver has less margin to distinguish a clean "1" from "0". The result is a poorer signal that requires assisting products (equalizers / retimers) or a shorter cable reach to maintain reliable transmission.

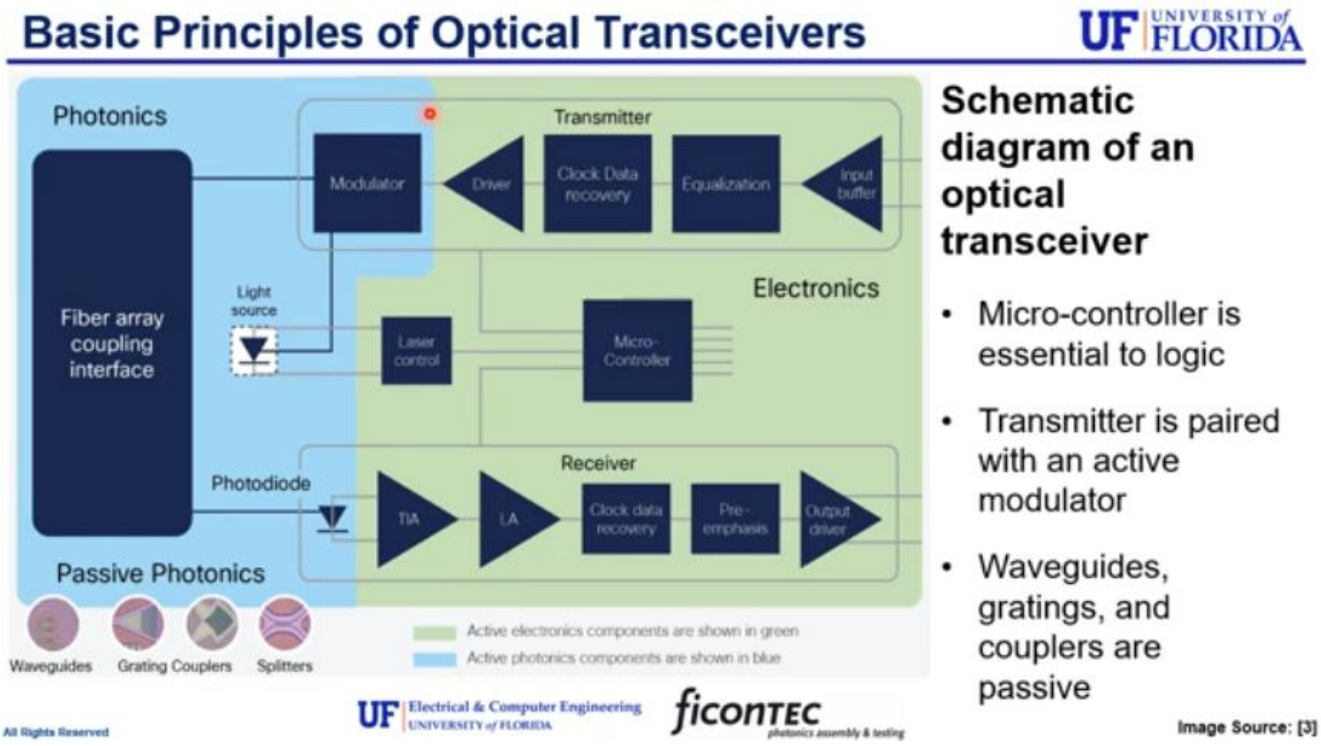
METRIC	COPPER (DAC)	OPTICAL (TRANSCEIVER)
Reach	<3m passive; 5-7m AEC	>50m to kilometres
Power consumption	Lowest (<1W; up to 12W AEC)	Higher (north of 15W; electro-optical conversion)
Latency	Lowest (direct)	Higher (encoding/ DSP)
Reliability	High (robust)	Lower (sensitive to heat/ RIN / aging)
Cost	Lowest	Higher (InP & SiPh complexity)

Active Electrical Cables (AECs) — a multi-hundred-million-to-billion-dollar market led by Credo, with Marvell also competing in this space — provide a temporary copper bridge, using integrated retimers to regenerate the signal and push reliable reach to roughly 7 metres at 800G (Blackwell B200 builds). But that reach collapses as data rates climb, falling to under ~3 metres at 1.6T (Blackwell Ultra, Rubin builds). As we approach 3.2Tbps data rates and beyond, the transition to optics becomes an architectural mandate.



Source: AI-generated (ChatGPT, OpenAI, May 2026). For illustrative purposes only.

Today, the industry's primary approach with optics is using **pluggable transceivers,** which are standalone modules that plug into a network switch or server. They resemble a thumb drive and are used to convert electrical signals to light and vice versa for data transmission. Transceivers have been in use for decades since the internet revolution of the 2000s and have been increasingly used at scale-out distances given the limitations of copper.



Source: University of Florida

The pluggable "power tax"

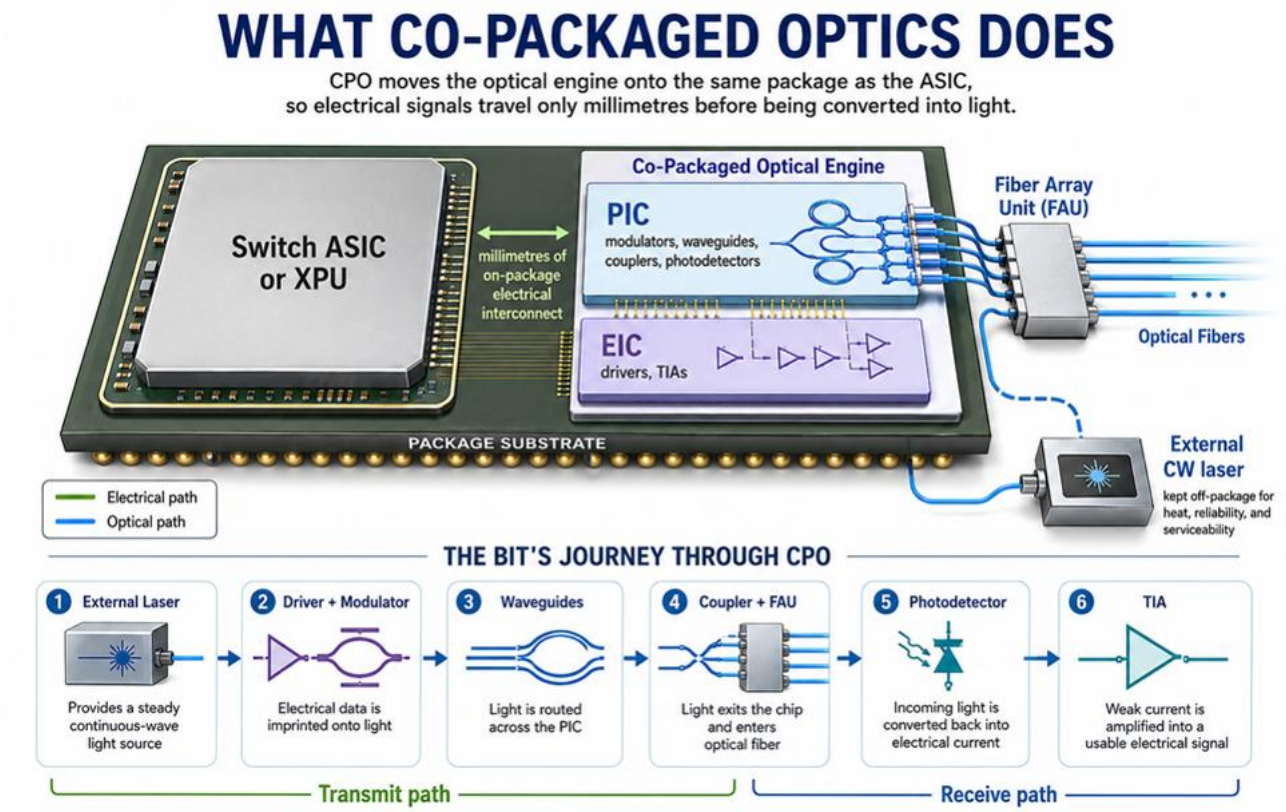
The issue with pluggable transceivers is their **power consumption**; each 1.6T transceiver uses up to 30W and each GPU in a server is attached to up to 6 transceivers, depending on connection architecture. Since a Rubin GPU consumes 1.8 – 2.3kW of power, transceivers take up to 180W per GPU, equivalent to 8-10% of the GPU's power. At the data centre level, transceivers take up 4-5% of an entire data centre's power budget. At a standard cost of $1 million per MW-year, a 1 GW data centre spends $40–50 million annually just to power its transceivers.

~30W	~180W	4–5%	$40–50m
PER 1.6T TRANSCEIVER	PER GPU · 8–10% OF GPU POWER	OF DATA-CENTRE POWER BUDGET	ANNUAL BILL, 1 GW DATA CENTRE

The power consumption of transceivers is likely to scale linearly with the power consumption of XPUs, resembling a "power tax" that the industry is trying to reduce through different optical architectures. Despite competing proposals for Linear Pluggable Optics (LPO) and Linear Receive Optics (LRO), major industry vendors like NVIDIA and Broadcom are settling on Co-Packaged Optics (CPO) as the architectural standard for next-generation AI data centre networking.

02 WHAT IS CO-PACKAGED OPTICS?

Moving the optical engine onto the package



Source: AI-generated (ChatGPT, OpenAI, May 2026). For illustrative purposes only.

Co-Packaged Optics (CPO) refers to integrating the **Optical Engine** — the components that convert between electrical signals and light — directly onto the same package substrate as the switch ASIC or XPU, instead of housing them in a separate pluggable module. The electrical signal then travels only millimetres of on-package interconnect before it is turned into light, rather than through tens of centimetres of Printed Circuit Board (PCB) a pluggable requires. The optical engine itself is built around two co-designed dies: a **Photonic Integrated Circuit (PIC)**, which carries the optical components that generate, route, and detect light, and an **Electronic Integrated Circuit (EIC)**, which carries the high-speed electronics that drive and read those optical components.

The bit's journey, component by component

Light source (CW laser). Every link begins with a continuous-wave laser supplying raw optical power - a constant, unmodulated beam. Silicon can guide and modulate light but cannot lase efficiently, so light generation must come from direct-bandgap III-V materials such as Indium Phosphide (InP).

Modulator. Where electrical data is imprinted onto the light. A driver in the EIC varies an electrical signal across the modulator, which switches the passing beam on and off (or shifts its phase) to encode 1s and 0s. Three designs compete: Mach-Zehnder (MZM, physically large but tolerant), micro-ring (MRM, tiny and low-power but wavelength-sensitive), and electro-absorption (EAM, compact, fast, but narrower temperature and window). CPO favours compact MRM/EAM because dozens of channels must fit into a tiny footprint beside the ASIC.

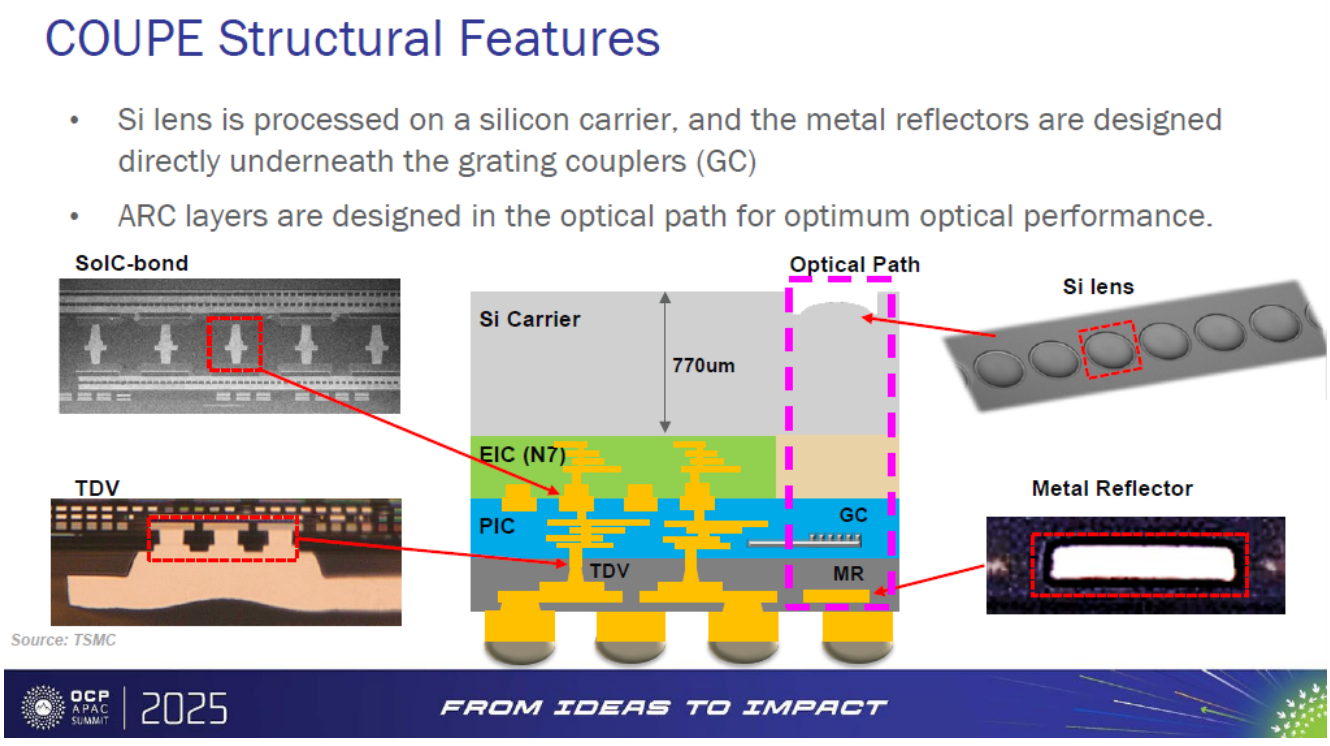
Waveguide. Once encoded, light travels across the chip through waveguides - microscopic channels etched into silicon guide photons much as a copper trace guides electrons. Silicon is low-loss at the relevant infrared wavelengths - the core reason silicon photonics (SiPh) is the scalable platform for CPO.

Coupler & Fibre Array Unit (FAU). Light then leaves the chip and enters the optical fibre that carries it onwards. A coupler bridges the size and index mismatch between waveguide and fibre – either through a grating coupler (vertical) or edge coupler (sideways). The FAU holds many fibres in precise alignment so an entire array of channels connects at once.

Photodetector & TIA (receive). At the far end the process runs in reverse: light strikes a photodetector producing a faint current, which a transimpedance amplifier (TIA) in the EIC boosts into a clean signal. Drivers and TIAs sit right beside the PIC - keeping the analog path short is exactly what preserves CPO's power and signal-integrity advantages.

The same building blocks appear inside a conventional pluggable transceiver; what makes CPO distinct is the physical co-location, which shortens the electrical path and removes the power-hungry DSPs and retimers that pluggables need to push signals across the board.

A worked example – TSMC COUPE



Source: TSMC (OCP 2025)

These are the generic building blocks; vendors implement them differently. TSMC's Compact Universal Photonics Engine (COUPE) is one prominent implementation: it 3D-stacks the EIC directly on top of the PIC using TSMC's SoIC bonding - rather than placing the two dies side by side - draws light from an external laser, and uses a grating-coupler design for fibre attach.

03 ENABLING THE TRANSITION

Four converging structural drivers

The move away from pluggable transceivers to Co-Packaged Optics (CPO) is enabled by four converging structural drivers: (1) a step-function reduction in optical-link power, (2) the maturation of chiplet architecture and advanced packaging, (3) Silicon Photonics (SiPh) as the integration platform that CPO depends on more critically than pluggables, and (4) emerging field reliability data that has begun to flip the historical assumption that pluggables are more reliable than CPO.

Power Efficiency. Power consumption drops from ~25–30W per 1.6T pluggable transceiver to ~9W per 1.6T CPO optical engine, roughly a **65–70% reduction**. This is 28–35MW saved for our 1GW data centre example earlier, or $28–35mn/year. The saving comes from two compounding effects: shortening the electrical path from centimetres of lossy PCB trace to millimetres on-package, which in turn eliminates the need for the power-hungry subcomponents like Digital Signal Processors (DSPs) and retimers that pluggables require to compensate for that loss.

Chiplet & Advanced Packaging Maturity. Instead of relying on a single large monolithic die, modern AI and networking systems increasingly use specialized chiplets (logic, memory, I/O, and now optical engines) integrated within the same package. This is enabled by advanced packaging technologies such as 2.5D interposers, redistribution layers, and high-density die-to-die interconnects, which allow chiplets to communicate at high bandwidth and low latency as if they were part of a monolithic system. Without this packaging maturity, co-locating an optical engine next to a switch ASIC at production yield would not be commercially viable.

Silicon Photonics as the Integration Platform. SiPh is not unique to CPO — it is already used in modern pluggables — but it is the substrate technology that makes CPO commercially scalable. As a platform, SiPh combines three strengths that III-V optical technologies (InP, GaAs) cannot match: (1) high integration density, with modulators, detectors, and waveguides fabricated on a single SiPh die; (2) process compatibility with mainstream foundry and advanced-packaging flows; and (3) access to the cost curve and capacity of established 200/300mm wafer fabs (TSMC, GlobalFoundries, Samsung, STMicro). Pluggables can use either III-V or SiPh because their form-factor and per-port-cost envelopes are forgiving. CPO — by definition co-packaged with compute or switch silicon — cannot, and the dependence on SiPh deepens with each CPO generation as port counts rise and integration tightens.

CPO Evaluation Infrastructure - Updated March' 26

Optics	Operating Temperature	Device Hours (400G)	MTBF
2x400G FR4 pluggable	40°C	~8M	0.71M
CPO Phase 1	40°C	>40M	1.47M
CPO Phase 1 (excluding PLS issue*)	40°C	>40M	8.2M (>10X improvement)
CPO Phase 1 (non-serviceable)	40°C	>40M	>20M
CPO Phase 2 (non-serviceable)	Room	>50M	Too Few Failures

* PLS issue isolated to laser driver circuit SMT component

Data shows that CPO ports are more reliable than pluggable module ports, potentially due to:

- Reduced number of interfaces and deeper level of integration
- Flexibility in co-design of the system with improved operating condition for key components (ie lasers)
- Integration of optics within the platform allows system level test and screening in the manufacturing line
- Reduced human intervention

Field serviceable PLS modules improve deployed reliability and decrease blast radius concern

Meta

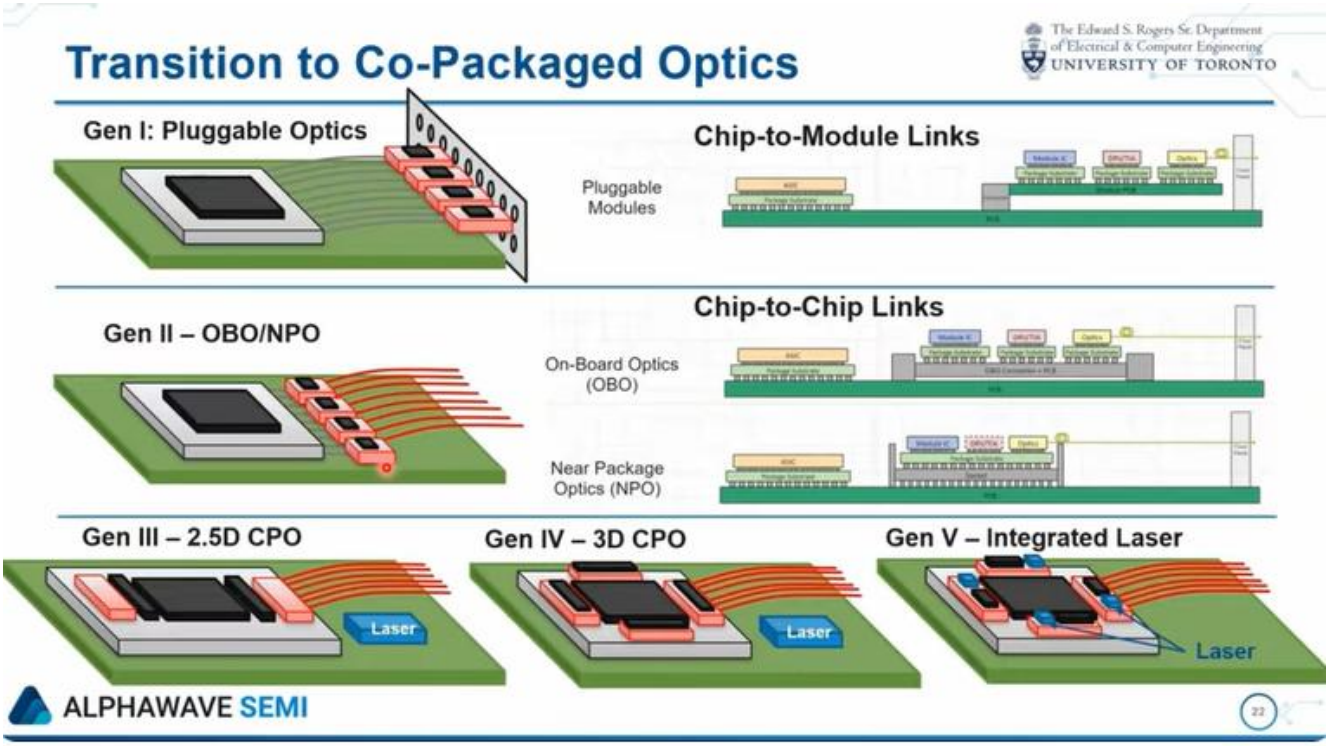
Source: Meta (OFC 2026)

Field-Proven Reliability (Meta Validation). Historically the main pushback against CPO was reliability: because the optical engine is co-packaged with the switch ASIC and/or XPU, a single optical failure could in principle take down the entire switch/XPU (the "compounded failure" or larger blast-radius concern). Two recent Meta data points have begun to invert that narrative. Phase 1 (October 2025): Broadcom and Meta reported one million cumulative 400G-equivalent port device hours of flap-free CPO operation in Meta's high-temperature lab characterization, alongside a 65% optics-power reduction vs. pluggables. Phase 2 (OFC 2026): Meta presented an extended ~90-million-hour reliability validation of its deployed CPO switch system, with second-generation hardware (Broadcom's Tomahawk5 Bailly) showing a Mean Time Between Failure (MTBF) roughly an order of magnitude better than the pluggable-based comparison fleet in the same trial. If Meta's data continues to hold at scale, reliability shifts from being CPO's biggest objection to one of its selling points — a meaningful catalyst for hyperscaler adoption decisions in 2026–2027.

04 THE CPO ROADMAP & ADOPTION PATH

Architecture generations

Two roadmaps are running in parallel. The first is the **architecture roadmap** — a generational progression toward tighter optical-electrical integration, framed by Alphawave Semi in 2022 as five generations of optical interconnect. The second is the **industry adoption** roadmap — the order in which the market commercializes each generation, which is being driven by where the physics, reliability, and economics work first.



Source: Alphawave Semi / University of Toronto

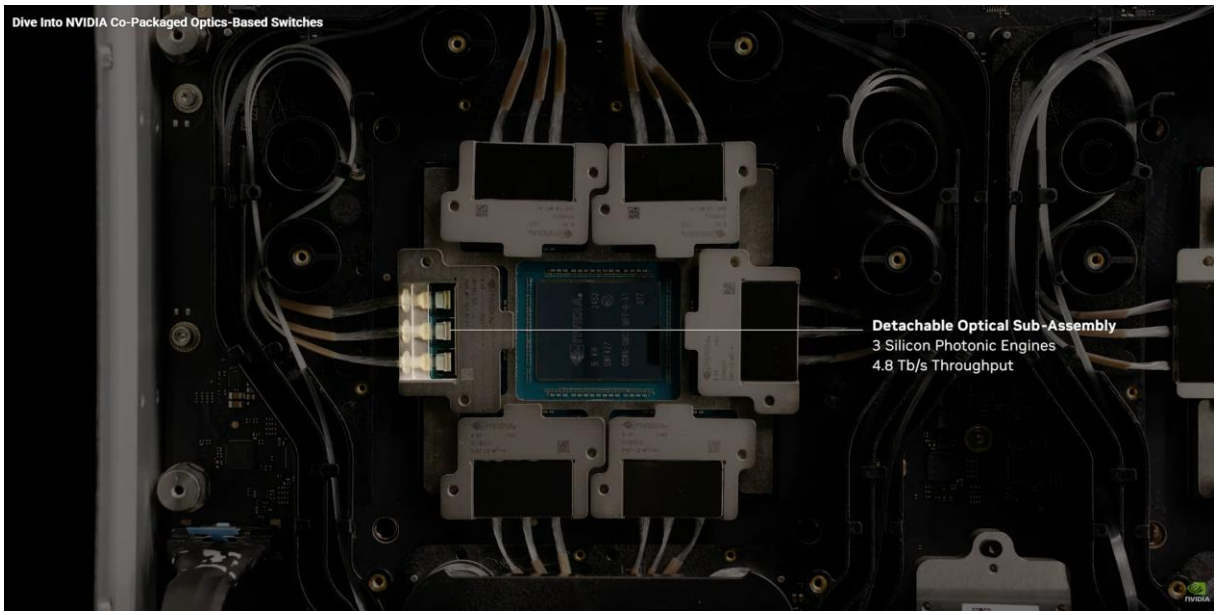
Gen I — Pluggable Optics: Today's baseline. Chip-to-module links via front-panel pluggable transceivers. 800G is the current deployed standard while 1.6T is ramping in 2026.

Gen II — On-Board Optics (OBO) / Near-Package Optics (NPO): The optical engine moves from the front-panel cage onto the same PCB as the ASIC, but still outside the package. Shorter electrical traces reduce loss and DSP requirements, but the engine is no longer hot-swappable. This generation has largely been skipped by Broadcom, while NVIDIA's Quantum-X800 Infiniband Q3450-LD switch arguably has a design in between Gen 1's "pluggable" and Gen 2's "NPO" despite being marketed as CPO as its 6 optical sub-assemblies are detachable from the switch chip, allowing replacement of the optical engines in the event of failure.

Gen III — 2.5D CPO: Inside the optical engine, the EIC and PIC sit side-by-side as two separate dies on a shared 2.5D interposer (CoWoS or equivalent), and that engine is co-packaged with the switch or compute ASIC. Electrical traces between the engine and the ASIC collapse from cm to mm. The laser is not integrated within the engine but designed into a module known as the External Laser Small Form-Factor Pluggable (ELSFP) that sits outside the package. In practice this generation is being largely skipped: placing the EIC and PIC side-by-side still leaves a longer electrical path between them than stacking does, so the industry is moving straight to Gen IV.

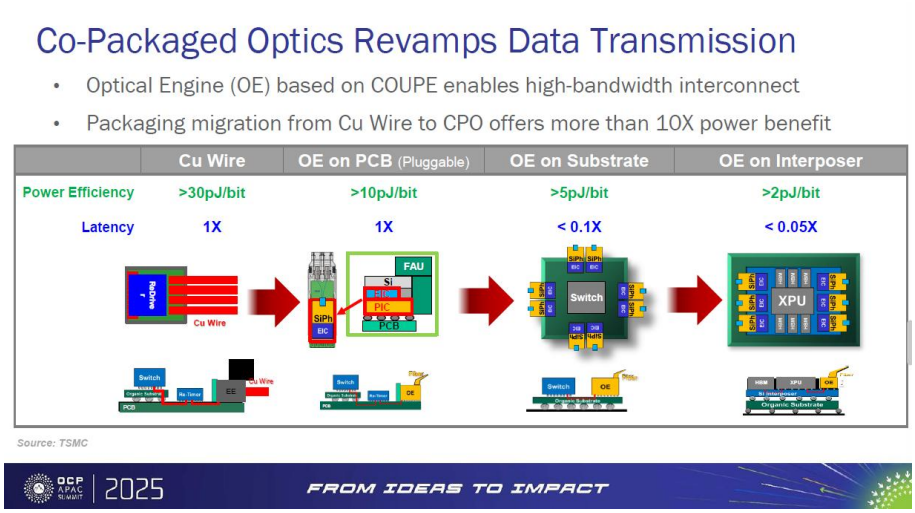
Gen IV — 3D CPO: The EIC is now 3D-stacked directly on top of the PIC rather than placed beside it. TSMC's COUPE is the leading implementation, bonding the EIC onto the PIC with its SoIC hybrid-bonding process. Stacking shortens the EIC-to-PIC electrical path further and shrinks the engine footprint, freeing package beachfront for additional I/O or HBM. The laser still sits outside the package via the ELSFP, which localises the failure-prone laser to a cheap, field-replaceable unit. This is the architecture NVIDIA's Spectrum-X Ethernet switches and Broadcom's Bailly/Davisson Ethernet switches are commercializing in 2026.

Gen V — Integrated Laser: The laser source itself is integrated into the package, rather than housed externally via an ELSFP. The architectural endpoint in theory, but currently blocked by reliability, thermal, and laser-output-power constraints. Remains a long-term target rather than a near-term commercial product.



Quantum-X800 InfiniBand switch with removable optical engines. Source: NVIDIA

Industry adoption: Switch first, XPU later



Source: TSMC (OCP 2025)

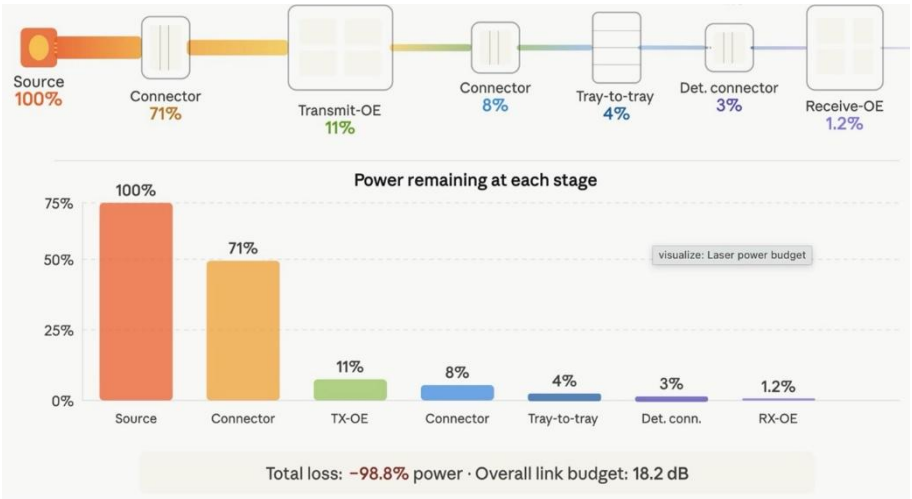
The industry is not adopting these generations in strict sequence. Two judgments are shaping the rollout:

1 **Switches before XPUs**

CPO is commercialized first on the switch side (NVIDIA Quantum-X / Spectrum-X, Broadcom TH5 Bailly and TH6 Davisson). On XPUs it is deferred: HBM stacks consume most of the package beachfront, leaving no perimeter for optical engines. Every commercialized CPO product to date is a switch, not an accelerator.

2 **Gen III/IV before Gen V**

Even within the switch, external-laser CPO beats an integrated laser - all rooted in failure-domain management. **Reliability:** a $50 integrated laser failure could otherwise brick a $50k ASIC. **Thermals:** lasers are very sensitive to heat, while ASICs run hot. **Power:** external laser modules deliver 100mW+ output vs. ~70mW on-package. This gives the laser link more insertion-loss budget.



Example of CPO link budget. Source: Semiengineering

CPO Development of key players

The primary vendors with a commercial CPO product ready in 2026 are NVIDIA and Broadcom; both continue to offer the pluggable variant alongside their CPO-ready switch.

Scale-Out Catalog	NVIDIA	NVIDIA	NVIDIA	NVIDIA	Broadcom	Broadcom
	Spectrum-6 (SN6810) (CPO)	Spectrum-6 (SN6800) (CPO)	Quantum-X800 (Q3400-RA)	Quantum-X800 (Q3450-LD) (NPO)	Tomahawk 5 (BCM78900) Bailly (CPO)	Tomahawk 6 (BCM78910) Davisson (CPO)
Protocol	Ethernet	Ethernet	InfiniBand (XDR)	InfiniBand (XDR)	Ethernet	Ethernet
Process Node	—	—	—	—	5nm	—
Switching Capacity (Tbps)	102.4	409.6	115.2	115.2	51.2	102.4
SerDes Count	512	2048	576	576	512	512
SerDes Speed (Gbps)	200	200	200	200	100	200
Max Port Speed	800 Gbps	800 Gbps	800 Gbps	800 Gbps	800 Gbps	1.6 Tbps
Port Configurations	128×800G / 512×200G	512×800G / 2,048×200G	144×800G (72 OSFP)	144×800G (direct MPO)	64×800G / 128×400G / 256×200G	64×1.6T / 128×800G / 256×400G / 512×200G
Key Platforms	SN6810 (single-ASIC)	SN6800 (quad-ASIC)	Q3400-RA (4U air-cooled)	Q3450-LD (4 switch ASICs)	Arista, Dell, various ODMs	OEM / ODM (H1 2026)
Availability	Late 2026	Late 2026	2026	2026	2024	Volume H1 2026
Status	Next gen (102.4T)	Next gen (409.6T)	Current gen (XDR 800G)	Next gen (CPO InfiniBand)	Current gen (51.2T)	Next gen (102.4T)
Switch Size (RU)	2U	5U	4U	4U	4U	TBA
External Laser Source	16	64	N/A	18	TBA	TBA
# Switch ASICs	1	4	4	4	1	1
Optical Engine Count	32 (3.2T)	128 (3.2T)	N/A	72 (1.6T)	8 (6.4T)	16 (6.4T)

Source: Company, collated by Swaen Capital

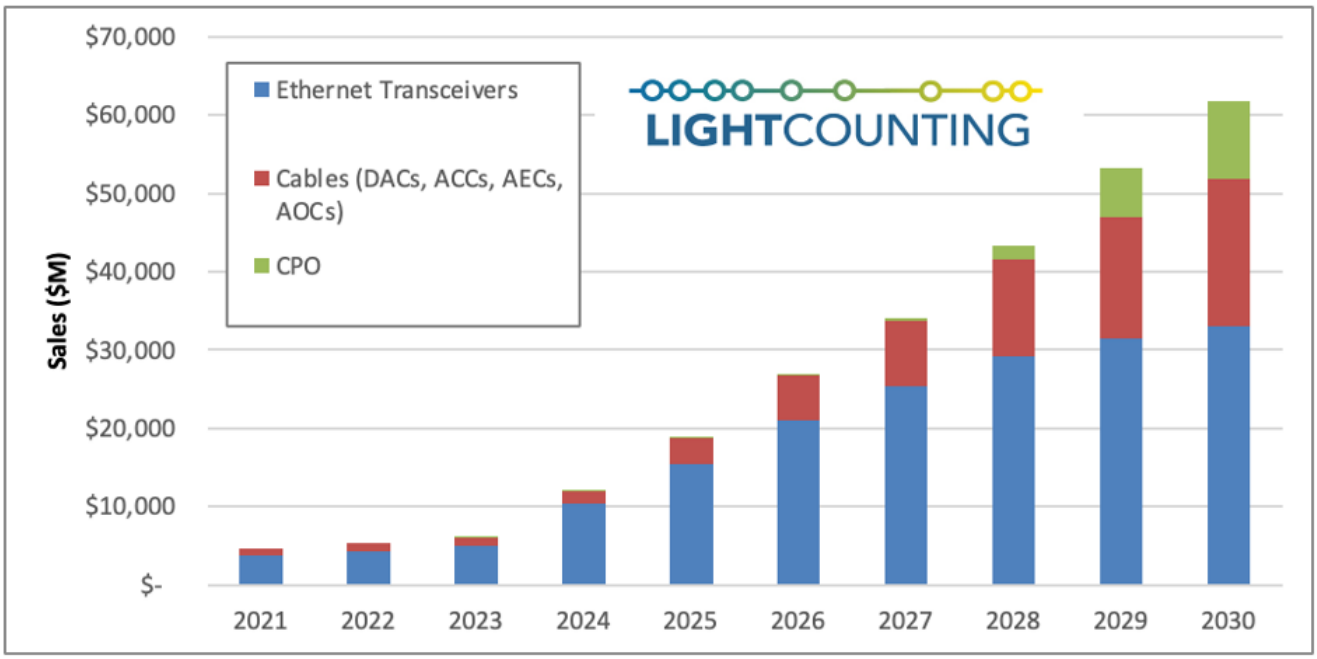
Marvell spans both switch and XPU: its first CPO switch demo (TX9190) came at OCP 2025 with SENKO, Jabil and Mikros; in February 2026 it acquired Celestial AI (CPO for XPUs via Photonic Fabric), and its Teralynx T100 ASIC is sampling with CPO and co-packaged-copper options. In March 2024 **Ranovus and MediaTek** announced a 6.4Tbps integrated-laser (Gen V) co-development, but little follow-up suggests a shelved plan.

Since data rates are still predominantly 200Gbps/lane for the upcoming generation, CPO adoption today is driven less by necessity and more by each customer's trust in the technology's reliability. Regular copper cables and optical transceivers will still play a major role this decade. The next section sizes how that demand splits between pluggables and CPO.

05 THE CPO SUPPLY CHAIN

Sizing the prize

Figure 2: Sales of 100G and higher speed Ethernet transceivers, cables and CPO



Source: LightCounting (Dec 2025)

The optical transceiver market is roughly US$16bn in 2025, with the CPO market being <1% of market given its nascency. Independent forecasters put the broad market near US$60–65bn by 2030 — about a 4x increase, or ~30% CAGR. However, the scale of CPO penetration differs between forecasters, from under 20% of optics (LightCounting) to roughly 60% (TrendForce) depending on how much CPO penetrates into scale-up connectivity.

FORECAST	2030 OPTICAL MARKET	CPO / NPO SLICE	IMPLIED CPO PENETRATION	READ
LightCounting	>USD60bn (incl. copper cables)	~USD10-12bn	<20% of optics	Conservative – CPO in switch-side
Trendforce	~USD65bn (pluggables ~26bn + CPO/NPO)	>USD39bn (from ~USD0.1bn in 2025)	~60% of optics	Aggressive – CPO/NPO ramps as scale-up goes optical 2028-2029

Source: LightCounting (Dec 2025) and Trendforce (Jun 2026)

How to read the chain: from substrates to toolmakers

The CPO supply chain breaks into five areas. The first four build the optical engine from the substrate up — the wafers it is grown on, the photonic/electronic core at its heart, the laser that powers it, and the fibre-array unit that couples its light into glass — while the fifth, capital equipment, is the picks-and-shovels layer that fabricates and tests the rest. Each area below pairs a short description with its confirmed vendors and potential entrants, the latter highlighted in yellow.

1. Upstream wafers & substrates

The raw material the stack is grown on: photonics-grade silicon-on-insulator (SOI) for the photonic IC, and III-V compound substrates - indium phosphide (InP), gallium arsenide (GaAs) for the lasers, which are subsequently used for III-V wafers. Independent of transceiver architecture, these raw materials will be required to build a working optical engine. While SiPh as a material has been gaining share from III-V compound substrates as mentioned in Section 3, SiPh modules still rely on InP lasers as the light source. As such, both materials will continue to exist in future optical module builds. Amongst the list, Soitec holds a unique position by being the biggest photonics-SOI wafer supplier, while also licensing out their Smart Cut technology to peers for them to produce the same wafers to compete in the market.

Company	Ticker	How they fit (purpose)	Market Cap (USDmn)	P/E	P/B	YTD Return%	CY Profit Growth	CY+1 Profit Growth
Upstream wafers and substrates								
Soitec	SOIT.PA	Photonics grade SOI wafer - only qualified volume supplier today	4,922	N/A	3.2	419.2	-102%	2930%
Shin Etsu	4063.T	Photonics grade SOI wafer - Smart Cut Licensee + sub-scale volumes	87,228	24.8	3.0	51.1	22%	9%
GlobalWafers	6488.TWO	Photonics grade SOI wafer - Smart Cut Licensee + sub-scale volumes	14,571	26.6	4.9	148.8	32%	37%
JX Advanced Metals	5016.T	III-V substrate for lasers	27,332	29.3	5.9	143.2	-6%	12%
Sumitomo Electric	5802.T	III-V substrate for lasers	60,073	17.7	3.5	101.4	-9%	19%
AXT	AXTI.O	III-V substrate for lasers	5,097	N/A	15.8	376.5	-193%	158%
Yunnan Germanium	002428.SZ	III-V substrate for lasers	11,840	1029.2	54.7	252.4	N/A	N/A
Freiberger	Private	III-V substrate for lasers	N/A	N/A	N/A	N/A	N/A	N/A
Landmark	3081.TWO	InP epi wafer for laser device makers	6,297	132.4	47.0	272.8	311%	109%
VPEC	2455.TW	InP epi wafer for laser device makers	2,318	51.2	20.0	162.7	81%	65%
Sumitomo Electric	5802.T	InP epi wafer for laser device makers	60,073	17.7	3.5	101.4	-9%	19%
IQE	IQE.L	InP epi wafer for laser device makers	868	N/A	5.4	896.0	-38%	-65%
IntelliEpi	4971.TWO	InP epi wafer for laser device makers	664	188.4	10.0	74.2	409%	51%
EPiHouse	Private	InP epi wafer for laser device makers	N/A	N/A	N/A	N/A	N/A	N/A

Source: LSEG, Swaen Capital

2. Photonic / Electronic core (PIC+EIC)

The heart of the optical engine. The photonic IC (PIC) holds the waveguides, modulators and photodetectors that convert electrons to light and back; the electronic IC (EIC) is the CMOS driver/TIA that runs them. The two can be built **monolithically** (PIC and EIC on one wafer) or — now the mainstream path — **heterogeneously**, fabbed in separate foundries and then 3D-bonded.

While TSMC has a first-mover advantage with the biggest customer onboard (NVIDIA) and owns the full stack (PIC fab, EIC fab, SoIC-X packaging technology, Si-carrier, PDK), they are not necessarily the most leveraged to CPO given their broad foundry exposure. Additionally, credible challengers that own a portion of the stack are coming in to compete - Tower's wafer bonding tech and GlobalFoundries' recent SCALE CPO announcement moves them closer to being the next full stack platform. The pursuits of Nokia, Intel and Scintil Photonics also suggest that Gen 5 architecture (integrated laser) is seeing interest in commercial development.

Company	Ticker	How they fit (purpose)	Market Cap (USDmn)	P/E	P/B	YTD Return%	CY Profit Growth	CY+1 Profit Growth
Photonic / Electronic core (PIC + EIC)								
TSMC	2330.TW	Provides TSMC COUPE, a major manufacturing platform for CPO, inclusive of various manufacturing procedures like producing the EIC and PIC themselves with their CMOS and SiPh foundry capabilities, EIC-on-PIC bonding (SoIC-X)	1,957,376	23.4	10.6	54.8	48%	27%
Tower Semiconductor	TSEM.O	Preferred SiPh foundry partner; introduced CPO-level 3D wafer-bonding in Nov2025, potential PIC+packaging	31,890	N/A	10.7	140.7	47%	72%
Global Foundries	GFS.O	SiPh foundry; Acquired Singapore's AMF in Nov2025 to grow SiPh; launched SCALE CPO optical module platform 4 May 2026, moving toward integrated offerings	45,756	22.0	4.0	138.8	5%	33%
ST Microelectronics	STM	SiPh foundry capability; partnership with Amazon for PIC100, their SiPh platform	66,093	144.2	3.6	180.4	127%	99%
UMC	UMC	SiPh foundry; licensed imec iSiPP300, currently risk production	70,702	14.8	5.1	233.3	26%	12%
Rain Tree Photonics	Private	SiPh optical engine designer	N/A	N/A	N/A	N/A	N/A	N/A
CompoundTek	Private	SiPh foundry capability	N/A	N/A	N/A	N/A	N/A	N/A
DNeX	DNEX.KL	60% owner of SilTerra, a Malaysia-based foundry expanding their SiPh profile	383	N/A	1.2	41	- 1	0
Samsung	005930.KS	Targets turnkey CPO service in 2029	1,410,734	18.2	4.7	159.1	549%	38%
Intel	INTC.O	Showcased Monolithic Optical Compute Interconnect (OCI) technology with on-chip DWDM laser	664,839	N/A	6.0	258.5	185%	44%
Nokia	NOK	Monolithic InP PIC (ICE-D) with lasers built into the PIC - architectural challenge to Gen 3/4.	78,740	52.2	3.2	115.8	21%	19%
Scintil Photonics	Private	Augmented-SiPh laser-on-PIC (LEAF Light) integrating III-V lasers onto the PIC; challenger to SiPh-PIC + external DFB Gen 3/4 architecture. Using Tower Semi's SiPh platform	N/A	N/A	N/A	N/A	N/A	N/A

Source: LSEG, Swaen Capital

3. ELS – External Laser Source

Today's implementation of CPO moves the laser off the hot optical engine and out to a replaceable module on the faceplate, because lasers degrade with heat. The External Laser Source is a high-power continuous-wave laser that pipes raw light into the engine over fibre — in effect a 'light battery' feeding the modulators.

Currently, Lumentum and Coherent are the named sources, each backed by a ~US$2bn Nvidia investment that signals strategic lock-in with Lumentum having the technological edge on laser capability. Multiple laser makers who were supplying for pluggables are now in the sampling stages for the high-power variant that is suitable for CPO.

Company	Ticker	How they fit (purpose)	Market Cap (USDmn)	P/E	P/B	YTD Return%	CY Profit Growth	CY+1 Profit Growth
ELS - External Laser Source								
Lumentum	LITE.O	Ultra-high-power single DFB (~350 mW @50C, 1311 nm) in the ELSFP - workhorse source for Quantum-X Q3450.	65,549	254.6	20.3	128.6	393%	140%
Sumitomo Electric	5802.T	Merchant CW DFB laser chips feeding ELS modules; named Nvidia SiPh ecosystem partner.	60,301	17.7	3.5	96.7	-9%	19%
Coherent	COHR.K	EML lasers for 800G/1.6T pluggables; sampling 400mW CW lasers	76,788	N/A	7.2	112.7	89%	60%
Broadcom	AVGO.O	EML lasers for 800G/1.6T pluggables; direct-drive CPO optionality.	1,817,729	77.6	20.7	10.8	68%	64%
Mitsubishi Electric	6503.T	EML lasers for 800G/1.6T pluggables; direct-drive CPO optionality.	79,671	25.2	2.8	28.6	20%	11%
Furukawa Electric	5801.T	Merchant DFB chips (volume today for pluggables); new Iwate ELS-grade plant ramps 2026-28.	20,395	27.9	7.8	377.1	18%	37%
Applied Optoelectronics	AAOI.O	400 mW narrow-linewidth CW pump laser sampling; volume late-2026 - challenger to Lumentum UHP DFB.	11,793	N/A	10.5	321.6	-615%	455%
Ayar Labs	Private	DFB laser array / multi-wavelength ELS (SuperNova, ~16 lambda); demo/sampling	N/A	N/A	N/A	N/A	N/A	N/A
Innolume	Private	Quantum-dot mode-locked frequency-comb laser (24 ch @100 GHz); power-efficient future WDM ELS	N/A	N/A	N/A	N/A	N/A	N/A
Xscape Photonics	Private	Pumped nonlinear resonant comb laser (FalconX) for WDM CPO; sampling Mar-2026; Nvidia-invested.	N/A	N/A	N/A	N/A	N/A	N/A
Enlightra	Private	Resonant comb-laser research for WDM CPO; pre-revenue.	N/A	N/A	N/A	N/A	N/A	N/A
Iloomina	Private	Resonant comb-laser research for WDM CPO; pre-revenue.	N/A	N/A	N/A	N/A	N/A	N/A
Semtech	SMTC.O	InP gain chips / DFB die via HieFo (acquisition closed Mar-2026, integration starting).	14,763	NULL	25.7	115.1	50%	46%
Nokia	NOK	InP gain chip / DFB die from planned San Jose InP fab (target 2026/27).	79,500	52.2	3.2	115.8	21%	19%
DenseLight	Private	Vertically integrated InP laser fab with 100mW CW DFB laser	N/A	N/A	N/A	N/A	N/A	N/A
Lightmatter	Private	Guide DR liquid-cooled laser-NIC packing dozens of lasers; ELS-layer competitor, samples Q4-2026 (COMPUTEX 2026).	N/A	N/A	N/A	N/A	N/A	N/A

Source: LSEG, Swaen Capital

4. FAU – Fibre Array Unit

The part that couples light off the chip and into the fibre, consisting of a microlens array and a V-groove array that holds each fibre in exact alignment. Microns of misalignment can lead to signal insertion loss, which is why this tiny passive component is so hard to make.

Currently, Himax is the primary named source of the FAU optics block and V-groove for NVIDIA / TSMC COUPE, with FOCI doing final assembly. Contestability here deals with future architectural changes, such as with metalenses potentially replacing microlenses, or new partnerships outside of the primary NVIDIA / TSMC ecosystem.

Company	Ticker	How they fit (purpose)	Market Cap (USDmn)	P/E	P/B	YTD Return%	CY Profit Growth	CY+1 Profit Growth
FAU - Fiber Array Unit								
Himax	6488.TWO	Likely TSMC COUPE supplier: FAU optics block - glass microlens array and V-groove array	16,776	26.6	5.7	170.9	32%	37%
FOCI Fiber Optics	3363.TWO	Likely TSMC COUPE supplier: FAU final assembly - fiber load, optics-block attach and alignment	2,558	2928.1	14.1	52.6	394%	2282%
Browave	3163.TWO	NVIDIA Ecosystem partner - adjacent fiber-array / passive-optics player	2,274	64.1	22.5	126.6	22%	142%
TFC Optical	300394.SZ	NVIDIA Ecosystem partner - fiber-array / passive optics.	54,334	109.7	61.3	127.5	93%	46%
Advanced Fibre Resources	300620.SZ	NVIDIA Ecosystem partner - fiber-array / passive optics.	14,410	210.4	44.2	169.0	141%	40%
Senko	Private	NVIDIA Ecosystem partner - fiber-array / passive optics.	N/A	N/A	N/A	N/A	N/A	N/A
Sumitomo Electric	5802.T	NVIDIA Ecosystem partner - fiber-array / passive optics.	60,301	17.7	3.5	96.7	-9%	19%
Corning	GLW	Confirmed Broadcom supplier: Both FAU and fibre solutions	177,145	47.8	15.8	135.9	27%	33%
MetaOptics Technologies	METO.SI	Wafer-scale glass metalens optical I/O - alternative to the microlens array	145	N/A	18.6	-34.7	N/A	N/A
Metalenz	Private	UMC 40nm CMOS metasurface metalens - alternative to the microlens array	N/A	N/A	N/A	N/A	N/A	N/A
AuthenX	Private	Detachable 2D FAU with 12-inch CMOS meta-lens; alternative to microlens array	N/A	N/A	N/A	N/A	N/A	N/A
Largan Precision	3008.TW	Glass components for FAUs - debuted CPO components at COMPUTEX 2026	21,479	15.9	3.7	110.8	15%	6%

Source: LSEG, Swaen Capital

5. Capital equipment

The tools that fabricate the layers above, help with the packaging and assembly, and finally test equipment to ensure that everything works. These don't ship a CPO part; they enable everyone who does.

Of note is AIXTRON who holds an estimated 70–90% of Metal-Organic Chemical Vapour Deposition (MOCVD) for laser/InP epitaxy — a concentrated, indirect way to own laser-supply growth without picking a laser winner. Veeco's Lumina is a secondary supplier.

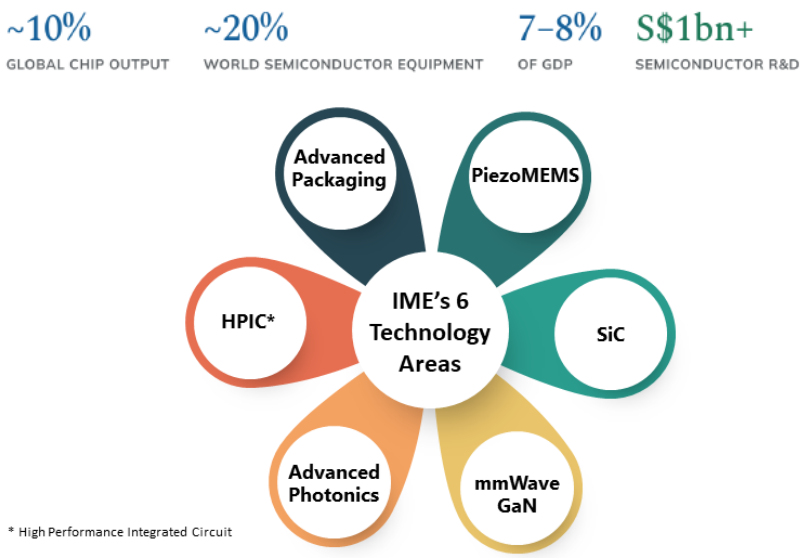
Company	Ticker	How they fit (purpose)	Market Cap (USDmn)	P/E	P/B	YTD Return%	CY Profit Growth	CY+1 Profit Growth
Capital equipment								
AIXTRON	AIXGn.de	MOCVD reactors for III-V (InP/GaAs) epi growth.	6,004	22.9	6.7	206.6	-2%	78%
Veeco	VECO.O	MOCVD reactors for III-V (InP/GaAs) epi growth.	4,605	48.9	5.2	164.0	29%	107%
ASMPT	0522.HK	Photonics packaging tools - die bonders, dispensers, alignment used at OSAT.	11,177	29.7	5.1	174.1	216%	49%
Kulicke & Soffa	KLIC.O	Photonics packaging tools - die bonders / alignment.	6,881	118.5	8.0	190.0	1520%	22%
All Ring	6187.TWO	Photonics packaging / assembly tools.	3,807	23.7	17.5	217.3	51%	73%
Shibuya	6340.T	Photonics packaging / assembly tools.	733	8.9	1.0	22.8	-10%	7%
Finetech	Private	Photonics packaging / alignment tools.	N/A	N/A	N/A	N/A	N/A	N/A
GKG Precision	301338.SZ	Photonics packaging / assembly tools.	3,725	70.3	14.8	159.2	100%	50%
RoboTechnik	300757.SZ	Photonics packaging / assembly tools.	16,518	N/A	68.7	183.0	-226%	238%
MPI	6223.TWO	E/O test equipment (wafer & module level) for COUPE OEs.	19,869	67.2	39.9	185.3	86%	88%
Teradyne	TER.O	E/O test equipment for COUPE OEs.	73,882	55.8	23.5	144.0	82%	33%
Keysight	KEYS.K	E/O test equipment for COUPE OEs.	61,533	36.4	9.7	77.2	37%	16%
FormFactor	FORM.O	E/O test / CPO probe for COUPE OEs.	11,596	83.6	11.0	166.7	91%	29%
Chroma ATE	2360.TW	E/O test equipment for COUPE OEs.	31,052	28.2	35.3	190.3	51%	43%
Advantest	6857.T	E/O test equipment for COUPE OEs.	138,079	39.5	27.6	53.3	31%	25%
Tokyo Electron	8035.T	E/O test equipment for COUPE OEs.	221,677	29.8	16.7	113.6	23%	25%
Hon Precision	7769.TW	E/O test equipment for COUPE OEs.	39,672	45.3	20.0	114.0	75%	72%
AEHR Test Systems	AEHR.O	Wafer-level burn-in test for SiPh	3,107	N/A	22.0	389.3	-162%	-261%
Pentamaster	PMAS.KL	Wafer-level test for SiPh	3,516	N/A	4.4	27.8	37%	28%

Source: LSEG, Swaen Capital

06 SINGAPORE'S PART IN CPO

Not where CPO is bought; increasingly where it is built

Singapore is not where co-packaged optics is bought, but it is increasingly one of the places it is built. The country produces roughly 10% of global chip output and around 20% of the world's semiconductor equipment, with the sector contributing close to 7–8% of GDP and over a fifth of manufacturing output.



*Source: A*STAR IME*

Singapore's role is best read not as a national champion of the whole CPO stack but as a **support layer**: a cluster of mostly private, often smaller companies enabling the larger international firms that manufacture here, knitted together by A*STAR's Institute of Microelectronics (IME), which has run a national silicon-photonics programme since 2007 and seeded many of the local names. Singapore is now investing over S$1bn in semiconductor R&D, with advanced photonics and advanced packaging as named priorities. The names below are grouped not by where they sit in the supply chain but by what they are to an investor.

The anchor — GlobalFoundries: One name carries the section. GlobalFoundries books over 40% of its non-current assets in Singapore - a larger fixed-asset base than in the US - and deepened that footprint in November 2025 by acquiring Advanced Micro Foundry (AMF), a SiPh pure-play spun out of A*STAR IME in 2017, becoming the largest pure-play SiPh foundry by revenue. The same month it signed a Master Research Collaboration Agreement with A*STAR to co-develop SiPh locally, and in May 2026 launched SCALE, its optical-module platform for CPO. GF is the one large, listed, demonstrably committed way Singapore's CPO build-out shows up in a portfolio. If GF's CPO endeavours take off, GF's Singapore base could become one of few scaled non-Taiwan, non-China manufacturing hubs for AI optical interconnects.

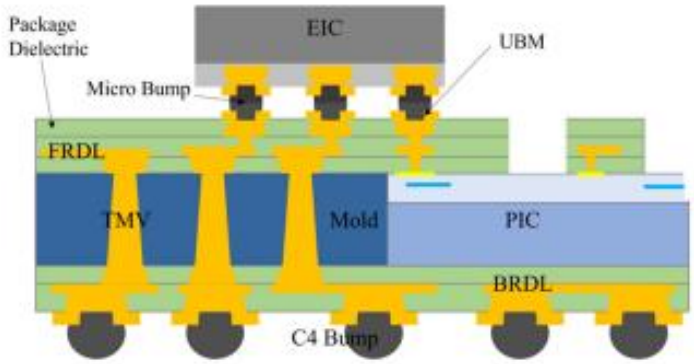


Fig. 1. Schematic of the FOWLP-based photonic engine.

*Source: Li et al., Journal of Lightwave Technology; Rain Tree Photonics / A*STAR / Advanced Micro Foundry*

The spin-off cluster: Around that anchor sits a set of smaller companies that grew out of Singapore's photonics base, each occupying a different slice of the engine: **CompoundTek** runs an 8-inch SiPh foundry and multi-project-wafer service; **Rain Tree Photonics**, an A*STAR IME spin-off, designs fabless optical engines spanning 400G to 1.6T, including a wafer-level-packaged ~1.8 Tbps engine for CPO and pluggables; **DenseLight**, founded out of NTU in 2000, fabs the InP high-power CW lasers that sit on the chain's tightest bottleneck. Lastly, **MetaOptics Technologies**, listed on SGX Catalist in Sep 2025, is the world's first pure-play metalens listed company. Its technology capability is closely tied to A*STAR, with licensed and co-developed patents and know-how. MetaOptics currently has a metalens CPO prototype, and as of April 2026 is undergoing sampling to enter the CPO supply chain.

The other backbone — Soitec: The substrate layer is partially a Singapore story and already in this report. Despite their French roots, Soitec, the dominant photonics-SOI supplier, runs its largest fab at Pasir Ris and books more than half of group revenue from Singapore. The Singapore fab is now undergoing qualification for photonic-SOI substrates with a long term goal of hitting 2 million wafers/year output.

On the fence — AEM and UMS: Two SGX-listed equipment names round out the picture without yet being in the chain. AEM Holdings has signalled it would begin co-design of a CPO-ready tester if its key customer commits to CPO in its architecture. UMS Integration has announced advanced-packaging capability, though the work shown to date points to HBM/DRAM rather than PIC/EIC packaging.

If GlobalFoundries' CPO endeavours take off, its Singapore base could become one of few scaled non-Taiwan, non-China manufacturing hubs for AI optical interconnects.

07 RISKS TO CPO ADOPTION

Three buckets to monitor

The preceding sections make the case for CPO while this one stress-tests it. We sort the risks into three buckets that behave differently: **substitutes**: rival technologies attacking the same bandwidth problem which displace CPO if they win; **execution risks**: frictions inside the CPO chain itself, which delay rather than displace; and **demand-side risks**, which determine how hard customers pull regardless of who wins the technology contest.

Substitutes

Better pluggables (LPO/LRO and next-generation DSPs): the pluggable ecosystem is not standing still. Each DSP generation improves energy efficiency, and Linear Pluggable Optics removes the DSP altogether which takes ~50% of a module's power, narrowing CPO's power advantage while preserving the two things hyperscalers value most: hot-swappable serviceability and multi-vendor sourcing. If 1.6T LPO qualifies at scale in 2026–27, the economic case for switch-side CPO compresses.

Active LED Cables (ALCs): Credo — having acquired micro-LED specialist Hyperlume in Dec 2025 and agreed to acquire SiPh firm DustPhotonics in April 2026 — is developing cables that replace lasers with micro-LEDs, targeting AEC-class reliability with optical reach of up to ~30 metres, and claims near-package variants at roughly one-third the power of CPO. Credo positions ALCs explicitly as a technology to extend the pluggable/cable ecosystem and delay CPO. The timeline keeps this a monitor-rather-than-act risk for now: sampling is planned for FY2027 with first revenue in FY2028, and no customers have been signed to date.

Co-Packaged Copper (CPC): the nearer-term threat to CPO's upside case. Instead of using Printed Circuit Boards (PCB) to route the electrical signal from switch/XPU package to the server faceplate, CPC routes it through copper cabling directly from a connector on the package substrate, extending copper's reach and power profile inside the rack. NVIDIA is pushing copper for scale-up out to 2027–28, and Marvell is building a CPC framework with cabling partners; 1.6T CPC solutions built on 200G lanes are expected within roughly two years, with 3.2T to follow. The effective range of CPC is limited since it is passive copper, but it outperforms the PCB with lower loss. CPC does not kill scale-out CPO, but it defers the "scale-up-goes-optical" scenario that underpins the most aggressive TAM forecasts.

Co-packaged Copper demo. Source: Samtec

THE INVESTMENT READ

Competitors are also publicly listed; should a competing technology be validated by a key customer, there could be an investment case for their company instead.

Execution Risks

Yield and known-good-die economics: a failed pluggable costs a ~US$1,500 module swap whereas a failed optical engine inside a package puts a far costlier switch and/or XPU assembly at risk. With CPO's all-in cost edge being quite minimal over pluggables, even minor yield losses can push costs above pluggables until packaging and optical Known Good Die testing matures.

Laser and InP capacity: the laser chain is the tightest physical bottleneck. Industry estimates call for InP capacity to expand roughly 12x over five years (Rosenblatt, May 2026), and MOCVD equipment lead times make that expansion slow to arrive — a constraint that caps the ramp regardless of demand.

Serviceability and blast radius: Meta's reliability data (Section 3) is one fleet at one hyperscaler. If it fails to replicate elsewhere, the historical objection — that a single optical failure strands an entire switch — reasserts itself.

Single-vendor stacks vs. multi-sourcing culture: buying CPO today means buying an integrated NVIDIA or Broadcom system. Hyperscalers have spent a decade enforcing multi-vendor supply chains, and some will resist the lock-in until OIF-style standards mature. Amazon's partnership with STMicroelectronics is one key example of this attempt to break free of vendor chokepoints.

Demand-side Risks

AI capex leverage: the entire CPO ramp is a derivative of AI cluster buildouts. A capex digestion phase at the hyperscalers, the biggest demand drivers of the buildout, pushes adoption further out by a product cycle.

Power-price geography: CPO's economics bind hardest where power is the binding constraint — Singapore's rationed grid is the canonical case, with its Green Data Centre Roadmap allocating new capacity partly on efficiency. Where power is cheap and unconstrained eg. the Gulf states, much of China; the dollar payback on optics-power savings weakens, and pluggables stay "good enough" for longer.

Two caveats keep this from being a veto on adoption: every operator still gains by reallocating watts from optics to revenue-generating compute, and adoption is partly supply-pushed — once NVIDIA and Broadcom make CPO the default high-end switch SKU, buyers inherit the architecture with the roadmap regardless of their power price.

08 GLOSSARY OF KEY TERMS

A quick reference, grouped by theme

ARCHITECTURES & LINK TYPES

CPO – co-packaged optics; optical engine integrated onto the same package as the switch ASIC or XPU.

NPO – near-packaged optics; optics on the same board, very close to the ASIC but not on-package.

Pluggable transceiver - hot-swappable optical module at the faceplate

LPO – linear pluggable optics; pluggable that removes the DSP, relying on host SerDes to save power.

LRO – linear receive optics; variant removing the DSP only on the receive path.

OPTICAL ENGINE COMPONENTS

Optical Engine (OE) - the PIC + EIC block converting between electrical and optical.

PIC - photonic die that generates, routes, modulates and detects light.

EIC - electronic die holding modulator drivers and TIAs.

Modulator (MZM / MRM / EAM) - imprints data onto light; large/robust, compact/low-power, or absorption-based.

Waveguide - on-chip silicon channel that guides light across the PIC.

Coupler (grating/ edge) - redirects light off the chip vertically or through the edge.

FAU – fibre array unit; precision assembly aligning multiple optical fibres against a photonic chip's couplers.

Photodetector I TIA - converts light back to current and boosts it to a usable signal.

CW Laser/ ELS - steady unmodulated source; ELS is the off-package module housing it.

MATERIALS & PACKAGING

SiPh - CMOS-compatible platform for optics on silicon at wafer scale.

InP / III-V - direct-bandgap compounds needed for efficient lasing, which silicon cannot do.

SOI - silicon-on-insulator wafer; the base for silicon photonics.

SoIC / CoWoS - TSMC advanced packaging for 3D stacking and 2.5D integration.

SUPPORTING ELECTRONICS & METRICS

ASIC/ XPU - the switch chip or AI accelerator the optics serve.

SerDes - converts parallel data into the serial lanes feeding the optics.

DSP – Digital Signal Processor; power-hungry chip cleaning up signals in pluggables; largely eliminated in CPO.

Retimer - regenerates degraded electrical signals to extend reach.

Insertion loss - optical power lost at a junction (dB); a key CPO yield metric.

MTBF - mean time between failures; the reliability yardstick in the Meta validation

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